In re Patent Application of:
DEQUINA ET AL
Serial No. **10/725,764**
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In the Specification:

Please replace paragraph [028] beginning at page 13, with the following rewritten paragraph:

The timing diagrams of Figures 5A-5C detail the controlled turn-off of UFET 3 and the subsequent turn-on of LFET 4, after a high-to-low transition 501 in the PWM signal 500. In particular, as shown by broken lines 502, turn off of the UGATE drive to UFET 3 is initiated at 511 by the high-to-low transition 501 in the PWM waveform of Figure 5A. Thereafter the PHASE node and UGATE node are monitored by associated threshold circuits 140 -160 within the dead time controller 100. Specifically, in response to the UGATE voltage dropping to a voltage level that is a prescribed value above the phase voltage (e.g., on the order of 1.75 V above the PHASE voltage ~~(+12V)~~ (-12V), as shown at 511, a prescribed time out (e.g., 10 ns) is triggered, as shown by broken lines 521, whereupon the LGATE signal 520 is transitioned from low-to-high at 522, turning on the LFET 4.